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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,335	08/28/2003	Sailesh Kottapalli	Intel 2207/16369	6836

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EXAMINER	
KO, DANIEL BOKMIN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,335	KOTTAPALLI ET AL.	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the application filed on 8/28/2003. Claims 1-34 have been submitted for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-5, 9-14, 18-22, 26-30, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US Patent 6,324,634 B1), hereinafter simply Yoshioka, in view of Hattersley et al. (US Patent 5,341,485), hereinafter simply Hattersley.

Regarding claims 1, 10, 19, and 27, Yoshioka teaches a method, comprising:

executing a first thread (column 1, lines 51-65, Yoshioka discloses the synonym problem that created by each task in a multi-task. So, first thread is equivalent to a task) requiring a first valid virtual memory address representing a first physical memory address (column 3, lines 35-44);

searching a translation look-aside buffer for the first valid virtual memory address (column 3, lines 35-50);

retrieving a first translation upon failing to find the first valid virtual memory address (column 3, lines 45-50);

searching the translation look-aside buffer for the first physical memory address (Fig. 11, S12; column 3, lines 50-56; column 10, lines 9-22).

Yoshioka fails to teach an overwriting a translation in the translation look-aside buffer corresponding to the first physical memory address with the translation. Hattersley teaches overwriting a translation in the translation look-aside buffer corresponding to the first physical memory address with the translation (column 2, lines 14-32). At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Yoshioka with Hattersley. The motivation for doing so would have been an enhancement of performance of TLB and reducing the traffic to the TLB (See Hattersley, column 2, lines 39-45).

Regarding claims 2, 11, 20, and 28, Yoshioka teaches a method, further comprising executing a second thread (column 1, lines 51-65, Yoshioka discloses the

synonym problem that created by each task in a multi-task. So, second thread is equivalent to another task) requiring a third translation corresponding to the first physical memory address (column 2, lines 16-19).

Regarding claims 3, 12, Yoshioka teaches a method, wherein a multithreaded processor executes the first thread and the second thread (column 1, lines 51-65).

Regarding claims 4, 13, 21, and 29, Yoshioka teaches a method, wherein the multithreaded processor executes the first thread and the second thread using switch on event multithreaded processing (column 1, lines 55-65).

Regarding claims 5, 14, 22, and 30, Yoshioka teaches a method, wherein the multithreaded processor executes the first thread and the second thread using simultaneous multithreaded processing (column 2, lines 16-19).

Regarding claims 9, 18, 26, and 34, Yoshioka teaches a method further comprising: creating a first one-hot index associated with the first physical memory address; and validating the first valid virtual memory address using the first one-hot index (column 6, lines 7-10; column 9, lines 7-14).

2. Claims 6-8, 15-17, 23-25, and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US Patent 6,324,634 B1), in view of Hattersley

et al. (US Patent 5,341,485), and further in view of Kohn et al. (US Patent 5,265,227), hereinafter simply Kohn.

Regarding claims 6, 15, 23, and 31, Yoshioka combined with Hattersley teaches the limitations of these claims as set forth for claims 1-5, above. However, Yoshioka or Hattersley do not teach an appending the access rights. Kohn teaches appending the access rights (column 2, lines 48-64). At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Kohn with Yoshioka and Hattersley. The motivation for doing so would have been a reduction of overall time period for executing a given instruction within a microprocessor (See Kohn, column 2, lines 28-32).

Regarding claims 7, 16, 24, and 32, it is obvious to erasing the first set of access rights if the third translation does not match the first translation, because second thread overwrites the translation and the first set of access write related to the first thread is no longer used or needed.

Regarding claims 8, 17, 25, and 33, Yoshioka teaches a method, wherein a content addressable memory is used to search the translation look-aside buffer (See Yoshioka, column 12, lines 33-38).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Ko

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Reginald G. Bragdon

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